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10/796,189	03/10/2004	Isao Hasegawa	65933-067	2729

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EXAMINER	
ROY, SIKHA	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 05/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,189	HASEGAWA ET AL.	
	Examiner	Art Unit	
	Sikha Roy	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-18* is/are pending in the application.

4a) Of the above claim(s) *13 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/378,907.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0106,0306*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The Response, filed on March 15, 2006 has been entered and acknowledged by the Examiner.

Claims 15-18 are pending in the instant application.

Claims 13 and 14 have been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 10170955 to Ichimura et al., and further in view of U.S. Patent 5,962,916 to Nakanishi et al.

Regarding claim 15 Ichimura discloses (sections [0003] – [0005], [0021], [0031] – [0033] Figs.2, 9a, 9b, 15) a display apparatus comprising a liquid crystal device including an optical element having an anode (pixel electrode), luminous element and a cathode (counter electrode) formed on layered structure of wires wherein the layered structure of wires is provided in a contact hole formed in an insulating film comprised of first insulating film 18 of SiO_2 film of thickness 30 nm and second insulating film 19 of SiN of thickness of 370 nm. Ichimura further discloses the layered structure of wires

includes first metal layer made of refractory metal Ti, wiring layer made of Al and a second metal layer of Ti having thickness of 100 nm formed in this order.

Claim 15 differs from Ichimura in that Ichimura does not explicitly disclose the contact hole includes a step difference at a boundary between the first insulating layer and the second insulating layer caused by different etching rates of the first insulating and second insulating layers.

Nakanishi in the pertinent art of manufacturing of thin film transistors discloses (Figs. 3 and 4 column 4 lines 45-67, column 5 lines 11-25) on the polycrystalline silicon film 25 an insulating silicon oxide film 27 and on the silicon oxide film 27 a silicon nitride film 28 are formed. Nakanishi further discloses that the insulating film of silicon oxide 27 (29) has a faster etching rate with respect to hydrofluoric acid-based etchant than that of the silicon nitride film 28 and hence the width of the contact hole 30 formed in the insulating layers differ, resulting in a step difference at a boundary between the first insulating layer 27 (29) and second insulating layer 28 as shown in Fig. 4. Furthermore Nakanishi discloses (column 3 lines 50-65) because of different etching rates of silicon oxide and silicon nitride films, the shape of silicon nitride film assumes a tapered shape that broadens toward the upper layer so that the contact hole is formed having satisfactory step coverage for the electrode shape. This makes it possible to prevent the occurrence of contact failure between the electrodes and the semiconductor film and at the same time prevent degradation of the operating characteristics of the transistor so as a result improvement in manufacturing yield can be expected.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a step difference at a boundary between the first insulating layer and the second insulating layers caused by different etching rates as taught by Nakanishi in the contact hole of Ichimura for preventing contact failure of the source and drain electrodes formed through the contact hole.

Regarding claim 16 Nakanishi discloses in the Fig. 4 that the contact hole 30 is formed in such a manner that the second insulating layer 28 has a taper slower than that of the first insulating layer 27.

Regarding claim 17 Ichimura discloses the second insulating film is formed such that the thickness (370 nm) of the second insulating film is greater than that of the first insulating layer and is less than 600nm.

Regarding claim 18 Ichimura discloses the first metal layer of Ti (thickness 50 nm) is thicker than the first insulating layer (thickness 30 nm).

Claims 15, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,281,552 to Kawasaki et al. and further in view of U.S. Patent 5,962,916 to Nakanishi et al.

Regarding claim 15 Kawasaki discloses (Figs. 2A, 2C, column 8 lines 12-28, column 17 lines 20-30, column 18 lines 20-25,46, 47) a self-light emitting display panel including driving circuit portion comprising layered structure of wires in the circuits formed from thin film transistors and optical element (pixel portion) formed on the

layered structure of wires comprising anode (pixel electrode) 2027, luminous element (EL material) 2029 and a cathode 2030 (Fig. 15B). Kawasaki discloses circuit structure comprising a protective insulating film 150, an interlayer insulating film 151 and a contact hole wiring structure (152 – 156), the protective insulating film and the interlayer insulating film formed from different material selected from silicon nitride film, silicon oxide film, silicon nitride oxide film, the interlayer insulating film 151 being stacked on the protective insulating film 150 (constitute a lamination film). The contact holes reaching the source regions or the drain regions of the respective TFT's are formed to form source wirings 152 – 156. Kawasaki discloses the wiring structure (electrodes) comprising a three-layered laminated film structure consisting of first refractory metal layer of Ti, wiring layer formed on the first metal layer of Al film containing Ti and second refractory metal layer of Ti film having thickness of 150 nm.

Regarding claim 15 Kawasaki does not explicitly disclose the contact hole includes a step difference at a boundary between the first insulating layer and the second insulating layer caused by different etching rates of the first insulating and second insulating layers.

Nakanishi in the pertinent art of manufacturing of thin film transistors discloses (Figs. 3 and 4 column 4 lines 45-67, column 5 lines 11-25) on the polycrystalline silicon film 25 an insulating silicon oxide film 27 (29) and on the silicon oxide film 27 a silicon nitride film 28 are formed. Nakanishi further discloses that the insulating film of silicon oxide 27 (29) has a faster etching rate with respect to hydrofluoric acid-based etchant than that of the silicon nitride film 28 and hence the width of the contact hole 30 formed

in the insulating layers differ, resulting in a step difference at a boundary between the first insulating layer 27 and second insulating layer 28 as shown in Fig. 4. Furthermore Nakanishi discloses (column 3 lines 50-65) because of different etching rates of silicon oxide and silicon nitride films, the shape of silicon nitride film assumes a tapered shape that broadens toward the upper layer so that the contact hole is formed having satisfactory step coverage for the electrode shape. This makes it possible to prevent the occurrence of contact failure between the electrodes and the semiconductor film and at the same time prevent degradation of the operating characteristics of the transistor so as a result improvement in manufacturing yield can be expected.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a step difference at a boundary between the first insulating layer and the second insulating layers in the contact hole of Kawasaki as taught by Nakanishi for preventing contact failure of the source and drain electrodes formed through the contact hole.

Regarding claim 16 Nakanishi discloses in the Fig. 4 that the contact hole 30 is formed in such a manner that the second insulating layer 28 has a taper slower than that of the first insulating layer 27.

Regarding claim 17 Kawasaki discloses (column 7 lines 40-44, column 8 lines 12-14) the second insulating layer 151 is formed with thickness of 500-1500 nm, greater than the thickness of first protective insulating layer 150 having thickness in the range from 100-400nm.

Response to Arguments

Applicant's arguments filed March 3, 2006 with respect to claim 15 have been fully considered but they are not persuasive.

Referring to page 4 of applicants' remarks, the applicants allege that Examiner's conclusion that contact failure can be prevented because of the step difference formed at the boundary between the first insulating film (silicon oxide film) and second insulating film (silicon nitride film) caused by different etching rates in the contact hole is not supported by Nakanishi. The Examiner respectfully disagrees. Nakanishi discloses (Figs. 3 and 4 column 4 lines 45-67, column 5 lines 11-25) on the polycrystalline silicon film 25 an insulating silicon oxide film 27 (29) and on the silicon oxide film 27 a silicon nitride film 28 are formed. Nakanishi further discloses that the insulating film of silicon oxide 27 (29) has a faster etching rate with respect to hydrofluoric acid-based etchant than that of the silicon nitride film 28 and hence the width of the contact hole 30 formed in the insulating layers differ, resulting in a step difference at a boundary between the first insulating layer 27 and second insulating layer 28 as shown in Fig. 4. Furthermore Nakanishi discloses (column 3 lines 50-65) because of different etching rates of silicon oxide and silicon nitride films, the shape of silicon nitride film assumes a tapered shape that broadens toward the upper layer so that the contact hole is formed having satisfactory step coverage for the electrode shape. This makes it possible to prevent the occurrence of contact failure between the electrodes and the semiconductor film

and at the same time prevent degradation of the operating characteristics of the transistor so as a result improvement in manufacturing yield can be expected.

Hence the Examiner notes that there is valid motivation and factual basis of preventing contact failure of the source and drain electrodes formed through the contact hole for combining Ichimura (Kawasaki) with Nakanishi to include a step difference at a boundary between the first insulating layer and the second insulating layers in the contact hole of Ichimura (Kawasaki) as taught by Nakanishi and hence the rejection stands.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sikha Roy whose telephone number is (571) 272-2463. The examiner can normally be reached on Monday-Friday 8:00 a.m. – 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S.R.

Sikha Roy
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Karabi Guharay

KARABI GUHARAY
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